In the claims:

Please amend the claims as follows:

1. (Canceled)

2. (Previously Presented) A domino logic circuit comprising:

a pulldown circuit having a dynamic node;

a keeper connected to the pulldown circuit at the dynamic node; and

a source of a body bias voltage, the source of the body bias voltage being connected to the keeper to supply the body bias voltage to the keeper to bias the keeper;

wherein the body bias voltage is a reverse body bias voltage.

3. (Original) The domino logic circuit of claim 2, wherein the reverse body bias voltage is static.

4. (Original) The domino logic circuit of claim 3, further comprising a foot transistor for connecting the pulldown circuit to ground.

5. (Original) The domino logic circuit of claim 3, wherein the pulldown circuit is connected to ground without an intervening foot transistor.

6. (Previously Presented) The domino logic circuit of claim 2, wherein the source supplies the reverse body bias voltage such that the reverse body bias voltage alternates between two values.

7. (Original) The domino logic circuit of claim 6, further comprising a foot transistor for connecting the pulldown circuit to ground.

8. (Original) The domino logic circuit of claim 6, wherein the pulldown circuit is connected to ground without an intervening foot transistor.

9. (Previously Presented) The domino logic circuit of claim 34, wherein the body bias voltage is a forward body bias voltage.

10-15. (Canceled)

16. (Previously Presented) A domino logic circuit comprising:

a pulldown circuit having a dynamic node;

a keeper connected to the pulldown circuit at the dynamic node; and

a source of a body bias voltage, the source of the body bias voltage being connected to the keeper to supply the body bias voltage to the keeper to bias the keeper;

wherein source supplies the body bias voltage such that the body bias voltage alternates between a first forward body bias voltage value and a second reverse body bias voltage value.

17. (Original) The domino logic circuit of claim 16, further comprising a foot transistor for connecting the pulldown circuit to ground.

18. (Original) The domino logic circuit of claim 16, wherein the pulldown circuit is connected to ground without an intervening foot transistor.

19. (Withdrawn) A source of an alternating voltage for biasing a keeper, the alternating voltage alternating between a first supply voltage and a second supply voltage, the source comprising:

an output connected to the keeper;

an input for receiving a clock;

a first supply voltage circuit connected between the first supply voltage and the output to supply the first supply voltage to the output;

a second supply voltage circuit connected between the second supply voltage and the output to supply the second supply voltage to the output;

a first transistor, connected to the clock without inversion, for selectively activating the first supply voltage circuit in accordance with the clock;

an inverter, connected to the clock, for outputting an inverted clock; and

a second transistor, connected to the inverter, for selectively activating the second supply voltage circuit in accordance with the inverted clock.

20. (Withdrawn) The source of claim 19, further comprising a first node, a second node and a third node, wherein:

the first transistor is connected between the first node and ground and is gated by the clock;

the second transistor is connected between the second node and ground and is gated by the inverted clock;

the first circuit comprises a third transistor connected between the first supply voltage and the third node and a fourth transistor connected between the second supply voltage and the second node, the third and fourth transistors being gated in accordance with a signal from the first node;

the second circuit comprises a fifth transistor connected between the second supply voltage and the first node and a sixth transistor connected between the second supply voltage and the third node, the fifth and sixth transistors being gated in accordance with a signal from the second node; and

the output is connected between the third node and the keeper.

21. (Withdrawn) The source of claim 20 , wherein the output comprises a delay for supplying the first and second supply voltages to the keeper in a time-delayed manner.

22. (Withdrawn) The source of claim 21, wherein the delay is a non-inverting delay.

23. (Withdrawn) The source of claim 20, wherein the body bias generator further comprises a delay for delaying the clock to supply a delayed clock to the first and second transistors.

24. (Withdrawn) The source of claim 23, wherein the delay is a non-inverting delay.

25. (Withdrawn) The source of claim 19, further comprising a first node, a second node and a third node, wherein:

the first transistor is connected between the first node and ground and is gated by the clock;

the second transistor is connected between the second node and ground and is gated by the inverted clock;

the first circuit comprises a third transistor connected between the first supply voltage and the third node and a fourth transistor connected between the second supply voltage and the second node, the third and fourth transistors being gated in accordance with a signal from the first node;

the second circuit comprises a fifth transistor connected between the third node and the first node and a sixth transistor connected between the second supply voltage and the third node, the fifth and sixth transistors being gated in accordance with a signal from the second node; and

the output is connected between the third node and the keeper.

26. (Currently Amended) The domino logic circuit of claim 6, wherein the source supplies the reverse body bias voltage such that the reverse body bias voltage alternates between the two values in accordance with ~~an operational phase of~~ a clock signal applied to the domino logic circuit.

27. (Withdrawn) The domino logic circuit of claim 26, wherein the source comprises:

an output connected to the keeper;

an input for receiving a clock;

a first supply voltage circuit connected between the first supply voltage and the output to supply the first supply voltage to the output;

a second supply voltage circuit connected between the second supply voltage and the output to supply the second supply voltage to the output;

a first transistor, connected to the clock without inversion, for selectively activating the first supply voltage circuit in accordance with the clock;

an inverter, connected to the clock, for outputting an inverted clock; and

a second transistor, connected to the inverter, for selectively activating the second supply voltage circuit in accordance with the inverted clock.

28. (Withdrawn) The domino logic circuit of claim 27, further comprising a first node, a second node and a third node, wherein:

the first transistor is connected between the first node and ground and is gated by the clock;

the second transistor is connected between the second node and ground and is gated by the inverted clock;

the first circuit comprises a third transistor connected between the first supply voltage and the third node and a fourth transistor connected between the second supply voltage and the second node, the third and fourth transistors being gated in accordance with a signal from the first node;

the second circuit comprises a fifth transistor connected between the second supply voltage and the first node and a sixth transistor connected between the second

supply voltage and the third node, the fifth and sixth transistors being gated in accordance with a signal from the second node; and

the output is connected between the third node and the keeper.

29. (Withdrawn) The domino logic circuit of claim 28, wherein the output comprises a delay for supplying the first and second supply voltages to the keeper in a time-delayed manner.

30. (Withdrawn) The domino logic circuit of claim 29, wherein the delay is a non-inverting delay.

31. (Withdrawn) The domino logic circuit of claim 28, wherein the body bias generator further comprises a delay for delaying the clock to supply a delayed clock to the first and second transistors.

32. (Withdrawn) The domino logic circuit of claim 31, wherein the delay is a non-inverting delay.

33. (Withdrawn) The domino logic circuit of claim 27, further comprising a first node, a second node and a third node, wherein:

the first transistor is connected between the first node and ground and is gated by the clock;

the second transistor is connected between the second node and ground and is gated by the inverted clock;

the first circuit comprises a third transistor connected between the first supply voltage and the third node and a fourth transistor connected between the second supply voltage and the second node, the third and fourth transistors being gated in accordance with a signal from the first node;

the second circuit comprises a fifth transistor connected between the third node and the first node and a sixth transistor connected between the second supply

voltage and the third node, the fifth and sixth transistors being gated in accordance with a signal from the second node; and

the output is connected between the third node and the keeper.

34. (Currently Amended) A domino logic circuit comprising:

a pulldown circuit having a dynamic node;

a keeper connected to the pulldown circuit at the dynamic node; and

a source of a body bias voltage, the source of the body bias voltage being connected to the keeper to supply the body bias voltage to the keeper to bias the keeper;

wherein the source supplies the body bias voltage such that the body bias voltage alternates between two values; and

wherein the source supplies the body bias voltage such that the body bias voltage alternates between the two values in accordance with ~~an operational phase of~~ a clock signal applied to the domino logic circuit.

35. (Withdrawn) The domino logic circuit of claim 34, wherein the source comprises:

an output connected to the keeper;

an input for receiving a clock;

a first supply voltage circuit connected between the first supply voltage and the output to supply the first supply voltage to the output;

a second supply voltage circuit connected between the second supply voltage and the output to supply the second supply voltage to the output;

a first transistor, connected to the clock without inversion, for selectively activating the first supply voltage circuit in accordance with the clock;

an inverter, connected to the clock, for outputting an inverted clock; and

a second transistor, connected to the inverter, for selectively activating the second supply voltage circuit in accordance with the inverted clock.

36. (Withdrawn) The domino logic circuit of claim 35, further comprising a first node, a second node and a third node, wherein:

the first transistor is connected between the first node and ground and is gated by the clock;

the second transistor is connected between the second node and ground and is gated by the inverted clock;

the first circuit comprises a third transistor connected between the first supply voltage and the third node and a fourth transistor connected between the second supply voltage and the second node, the third and fourth transistors being gated in accordance with a signal from the first node;

the second circuit comprises a fifth transistor connected between the second supply voltage and the first node and a sixth transistor connected between the second supply voltage and the third node, the fifth and sixth transistors being gated in accordance with a signal from the second node; and

the output is connected between the third node and the keeper.

37. (Withdrawn) The domino logic circuit of claim 36, wherein the output comprises a delay for supplying the first and second supply voltages to the keeper in a time-delayed manner.

38. (Withdrawn) The domino logic circuit of claim 37, wherein the delay is a non-inverting delay.

39. (Withdrawn) The domino logic circuit of claim 36, wherein the body bias generator further comprises a delay for delaying the clock to supply a delayed clock to the first and second transistors.

40. (Withdrawn) The domino logic circuit of claim 39, wherein the delay is a non-inverting delay.

41. (Withdrawn) The domino logic circuit of claim 35, further comprising a first node, a second node and a third node, wherein:

the first transistor is connected between the first node and ground and is gated by the clock;

the second transistor is connected between the second node and ground and is gated by the inverted clock;

the first circuit comprises a third transistor connected between the first supply voltage and the third node and a fourth transistor connected between the second supply voltage and the second node, the third and fourth transistors being gated in accordance with a signal from the first node;

the second circuit comprises a fifth transistor connected between the third node and the first node and a sixth transistor connected between the second supply voltage and the third node, the fifth and sixth transistors being gated in accordance with a signal from the second node; and

the output is connected between the third node and the keeper.

42. (Currently Amended) The domino logic circuit of claim 16, wherein the source supplies the body bias voltage such that the body bias voltage alternates between the first forward body bias voltage and the second reverse body bias voltage in accordance with ~~an operational phase of~~ a clock signal applied to the domino logic circuit.

43. (Withdrawn) The domino logic circuit of claim 42, wherein the source comprises:

an output connected to the keeper;

an input for receiving a clock;

a first supply voltage circuit connected between the first supply voltage and the output to supply the first supply voltage to the output;

a second supply voltage circuit connected between the second supply voltage and the output to supply the second supply voltage to the output;

a first transistor, connected to the clock without inversion, for selectively activating the first supply voltage circuit in accordance with the clock;

an inverter, connected to the clock, for outputting an inverted clock; and

a second transistor, connected to the inverter, for selectively activating the second supply voltage circuit in accordance with the inverted clock.

44. (Withdrawn) The domino logic circuit of claim 43, further comprising a first node, a second node and a third node, wherein:

the first transistor is connected between the first node and ground and is gated by the clock;

the second transistor is connected between the second node and ground and is gated by the inverted clock;

the first circuit comprises a third transistor connected between the first supply voltage and the third node and a fourth transistor connected between the second supply voltage and the second node, the third and fourth transistors being gated in accordance with a signal from the first node;

the second circuit comprises a fifth transistor connected between the second supply voltage and the first node and a sixth transistor connected between the second supply voltage and the third node, the fifth and sixth transistors being gated in accordance with a signal from the second node; and

the output is connected between the third node and the keeper.

45. (Withdrawn) The domino logic circuit of claim 44, wherein the output comprises a delay for supplying the first and second supply voltages to the keeper in a time-delayed manner.

46. (Withdrawn) The domino logic circuit of claim 45, wherein the delay is a non-inverting delay.

47. (Withdrawn) The domino logic circuit of claim 44, wherein the body bias generator further comprises a delay for delaying the clock to supply a delayed clock to the first and second transistors.

48. (Withdrawn) The domino logic circuit of claim 47, wherein the delay is a non-inverting delay.

49. (Withdrawn) The domino logic circuit of claim 43, further comprising a first node, a second node and a third node, wherein:

the first transistor is connected between the first node and ground and is gated by the clock;

the second transistor is connected between the second node and ground and is gated by the inverted clock;

the first circuit comprises a third transistor connected between the first supply voltage and the third node and a fourth transistor connected between the second supply voltage and the second node, the third and fourth transistors being gated in accordance with a signal from the first node;

the second circuit comprises a fifth transistor connected between the third node and the first node and a sixth transistor connected between the second supply voltage and the third node, the fifth and sixth transistors being gated in accordance with a signal from the second node; and

the output is connected between the third node and the keeper.

50-51. (Canceled)

INTERVIEW SUMMARY BY APPLICANT

At the outset, the Applicants acknowledge with appreciation the courtesy shown by the Examiner during the telephone interview conducted March 9, 2006. During the telephone interview, the Applicants' representative proposed addressing the rejection of claims 26, 34 and 42 under 35 U.S.C. § 112, second paragraph, by amending the claims to recite that the body bias voltage alternates between the two values in accordance with the clock signal. The Examiner agreed that such an amendment would overcome that ground of rejection.

Regarding the rejection under 35 U.S.C. § 102(e) of the claims reciting the reverse body bias voltage, the Examiner asserted that the applied reference teaches doing just that in col. 7, lines 45-48. In response, the Applicants' representative reminded the Examiner of the previously submitted arguments that what is described in that part of the reference is impossible when applied to the keeper. The Applicants' representative offered to prepare and file a Declaration under 37 C.F.R. § 1.132 to that effect. The Examiner said that he would consider such a Declaration, but he cautioned that it should be written in such a manner that the present invention is not proved to be impossible as well.

Regarding the rejection of the claims reciting a reverse body bias voltage which alternates between two values, the Applicants' representative offered to amend the claims to recite that the voltage alternates between the two values in accordance with a clock signal. The Examiner could not find such a teaching in the reference, but instead indicated that he would consider such an amendment and possibly do an expanded search.

Finally, with regard to the body bias voltage which alternates between a first forward value and a second reverse value, the Examiner pointed to teachings in

column 7 of the reference for both types of body bias voltages and said that an alternation between the two could have been accomplished in the present invention. The Applicants' representative reminded the Examiner that what merely could have been done is not the same thing as what the reference teaches and offered to cite case law to that effect. The Examiner said that the Applicants should submit such arguments in the formal response and that he would consider them then.